AMENDMENTS TO THE CLAIMS

As indicated below, Applicant is amending Claims 1, 5, 7, 8, 14, 15, 18, 20, 21, 24, 28, 30 and 31 and is cancelling Claims 9–12, 22 and 32–40 without prejudice or disclaimer. Claims 2–4, 6, 16, 17, 19, 25–27 and 29 remain as originally filed, and new Claims 41–46 have been added.

1. (Currently Amended) A method of performing data string operations comprising:

routing a series of instructions to a general purpose microprocessor having a first execution unit for executing instructions;

analyzing said series of instructions so as to detect an instruction to perform a data string manipulation operation;

~~routing~~ forwarding said instruction to perform [[a]] the data string manipulation operation from said first execution unit to a second execution unit, wherein said second execution unit is separate from said first execution unit, ~~wherein said second execution unit~~ and receives an undecoded version of said instruction;

controlling read and write operations to and from external memory with said first execution unit via control circuitry and without intervention by said second execution unit, wherein said external memory is external to said general purpose microprocessor; and

controlling read and write operations to and from external memory with said second execution unit via said control circuitry and without intervention by said first execution unit.

2. (Original) The method of Claim 1, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

3. (Original) The method of Claim 2, wherein said second integrated circuit includes a bus interface unit in association with said second execution unit.

4. (Original) The method of Claim 2, wherein said second integrated circuit comprises a memory controller.

5. (Currently Amended) The method of Claim 4, wherein said act of ~~routing~~ forwarding said data string manipulation instruction to said memory controller comprises writing said data string manipulation instruction to an I/O address.

6. (Original) The method of Claim 5, wherein said I/O address is normally not used for I/O devices.

7. (Currently Amended) The method of Claim 1, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string manipulation instruction is present in said data cache.

8. (Currently Amended) The method of Claim 7, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string manipulation instruction.

9.–13. (Cancelled)

14. (Currently Amended) A processing system comprising:

an instruction fetch unit coupled to an external memory;

a first execution unit configured to receive, decode, and perform assembly language arithmetic and logic instructions received from memory via said instruction fetch unit;

a second execution unit in communication with said first execution unit, said second execution unit being configured to receive, decode, and perform assembly language string manipulation instructions received from memory via said ~~instruction fetch~~ first execution unit;

memory circuitry, external to said first and second execution units; and

a bus interface unit, coupled to said memory circuitry, said first execution unit, and said second execution unit, wherein said memory circuitry is configured to be alternatively controlled by said first execution unit and said second execution unit via said bus interface unit, wherein said first execution unit is configured to operate said memory circuitry independently of said second

execution unit, and wherein said second execution unit is configured to operate said memory circuitry independently of said first execution unit.

15. (Currently Amended) A method of performing data string operations comprising:

routing a series of individual assembly language opcodes to a general purpose microprocessor having a first execution unit for executing instructions;

analyzing said series of assembly language opcodes so as to detect an instruction to perform a data string manipulation operation;

~~routing~~ forwarding said instruction to perform [[a]] the data string manipulation operation from said first execution unit to a second execution unit, wherein said second execution unit is separate from said first execution unit, wherein said instruction comprises at least one individual opcode for performing [[a]] the data string manipulation operation, and wherein said second execution unit receives an undecoded version of said instruction;

controlling read and write operations to and from memory external to said general purpose microprocessor with said first execution unit via control circuitry and independent of said second execution unit; and

controlling read and write operations to and from said memory with said second execution unit via said control circuitry and independent of said first execution unit.

16. (Original) The method of Claim 15, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

17. (Original) The method of Claim 16, wherein said second integrated circuit comprises a memory controller.

18. (Currently Amended) The method of Claim 17, wherein ~~routing~~ forwarding said instruction to perform a data string manipulation operation to said second execution unit comprises writing said data string manipulation instruction to an I/O address.

19. (Original) The method of Claim 18, wherein said I/O address is normally not used for I/O devices.

20. (Currently Amended) The method of Claim 15, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string manipulation instruction is present in said data cache.

21. (Currently Amended) The method of Claim 20, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string manipulation instruction.

22.–23. (Cancelled)

24. (Currently Amended) A method of performing data string operations comprising:

routing a series of instructions to a general purpose microprocessor having a first execution unit for executing instructions on data independent of a second execution unit;

analyzing said series of instructions with said first execution unit so as to detect an instruction to perform a data string manipulation operation on said data; and

~~routing~~ forwarding with the first execution unit said instruction to perform [[a]] the data string manipulation operation to a second execution unit separate from said first execution unit, wherein said second execution unit receives an undecoded version of said instruction.

25. (Original) The method of Claim 24, wherein said first execution unit is on a first integrated circuit and wherein said second execution unit is on a second integrated circuit.

26. (Original) The method of Claim 25, wherein said second integrated circuit includes a bus interface unit in association with said second execution unit.

27. (Original) The method of Claim 25, wherein said second integrated circuit comprises a memory controller.

28. (Currently Amended) The method of Claim 27, wherein said act of ~~routing~~ forwarding comprises forwarding said data string manipulation instruction to said memory controller comprises writing said data string manipulation instruction to an I/O address.

29. (Original) The method of Claim 28, wherein said I/O address is normally not used for I/O devices.

30. (Currently Amended) The method of Claim 26, additionally comprising checking the content of a data cache to determine if at least a portion of a data string which is the subject of said data string manipulation instruction is present in said data cache.

31. (Currently Amended) The method of Claim 30, wherein modified cache lines present in said data cache which contain data forming at least a portion of said data string are written back to main memory before or during the execution of said data string manipulation instruction.

32.–40. (Cancelled)

41. (New) The method of Claim 1, wherein said analyzing is performed by said first execution unit.

42. (New) The method of Claim 1, wherein said analyzing said series of instructions further comprises detecting a second instruction to perform a non-string arithmetic or logical operation.

43. (New) The method of Claim 42, additionally comprising performing said second instruction to perform the non-string arithmetic or logical operation with said first execution unit.

44. (New) The method of Claim 1, wherein each instruction of said series of instructions is performed by only one of the first execution unit and the second execution unit.

45. (New) The processing system of Claim 14, wherein the first execution unit further comprises an instruction register and an instruction decoder.

46. (New) The method of Claim 15, wherein said analyzing is performed by said first execution unit.